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Multi-physics modeling in virtual prototyping of electronic packages—combined thermal, thermo-mechanical and vapor pressure modeling

X.J. Fan [a,*], J. Zhou [b], G.Q. Zhang [c]

[a] Philips Research USA, 345 Scarborough Road, Briarcliff Manor, NY 10510, USA
[b] Department of Mechanical Engineering, Lamar University, Beaumont, TX 77710, USA
[c] Eindhoven University of Technology, P.O. Box 513, WH 4.110, Eindhoven, The Netherlands

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Abstract

The realization of virtual prototyping of electronic packages depends on the capability and reliability of multi-physics modeling. This paper focuses on the methods and solutions of combined thermal and thermo-mechanical modeling. The package-level thermal behaviors for various kinds of packages are discussed first through the thermal simulation. The impact of internal package design on thermal performance is highlighted. Then the methods and solutions of combined thermal and thermo-mechanical modeling are addressed in detail. The strong interactions of thermal and mechanical simulations, as well as the trade-off between thermal and mechanical designs are discussed through two case studies. The benefit of moisture behavior modeling for the package design is also briefed in this paper.
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1. Introduction

In the recent years, driven by the ongoing trend of miniaturization and function integration, thermal, mechanical and thermo-mechanical design and qualification of electronic packages are drawing more attentions from both industries and academic communities [1,2]. It is mainly due to the facts that:

- Time-to-market is becoming one of the dominant factors determining the profitability of the microelectronic products. For mobile phone products, for example, the important part of the business profitability is realized in the first quarter of the market introduction.
- Thermo-mechanical reliability of microelectronics is one of the major concerns for industry. Currently, about 65% of all failures in electronic packages is related to thermo-mechanical problems [3]. This is expected to become even more critical for the future microelectronic products due to the continued trend of miniaturisation and function integration, which causes increased power dissipation, higher interconnection density and higher reliability demands.
- Most of the thermo-mechanical reliability problems originate from the product/process design phase. However, within electronics industry, the traditional thermo-mechanical design and qualification method (designing, building and testing of a multiplicity of physical prototypes) is still commonly used. This method is characterised by several iteration cycles of designing, building and testing physical prototypes,

* Corresponding author. Address: ATD Q&R, CH5-263, Intel Corporation, 5000 W. Chandler Blvd, Chandler, AZ 85226, USA. Tel.: +1-480-554-1308; fax: +1-480-554-7171.
E-mail address: xuejun.fan@ieee.org (X.J. Fan).

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and product reliability is only dealt with after physical prototyping.

Due to fierce competition, ever-increasing market drive and strengthening of environmental legislation, the traditional thermal, mechanical and thermo-mechanical design and qualification methods are no longer competitive. Therefore, there is a strong industrial demand to develop innovative thermal, mechanical and thermo-mechanical design and qualification methods for the development of further miniaturised electronic packages.

Virtual prototyping is a promising and emerging technology advance for product and process design and qualification. In the development of electronic packages a multi-disciplinary, multi-physics and multi-scale method should be followed. This includes electrical modeling, electro-magnetic modeling, thermal modeling and design, as well as the thermo-mechanical modeling. From a mechanical point of view, thermal and thermo-mechanical modeling (including the moisture related modeling) are two integrated elements.

This paper first presents an overview and simulation results of thermal behaviors of various electronic packages. Fundamental cooling mechanisms associated with different packaging technologies, including wire-bond, strap bonding, flip chip and ball grid array (BGA), are investigated. Then the interactions between thermal and thermo-mechanical simulations are addressed. Several case studies are provided to show how an optimized package design can be achieved through the combined thermal and thermo-mechanical modeling. In the last section of this paper, the simulation of the moisture-induced failures is briefed. As an integrated part of mechanical reliability analysis, the impact of the vapor pressure modeling during the reflow on the materials selection is discussed.

2. Package-level thermal behaviors: thermal simulation

The junction temperature of a semiconductor device must be kept in a specified temperature window. Usually the maximum junction temperature is set below 125 °C. The junction temperature depends on many factors, such as packaging design (interconnect and structure), board selection (material, structure and interface), heat sink attachment (heat sink design and interface materials), ambient conditions (ambient temperature and air flow speed), as well as the system integration. The package design plays a very important role in overall thermal management because it provides the first 'gate' for the heat dissipation from the silicon chips [4].

In Fig. 1, a series of the standard outline (SO) packages are considered to investigate the impact of the package design on the thermal behaviors. The original standard IC SO-8 (8 leads) package uses wires on the top of chip to connect all leads (Fig. 1a). The standard power MOSFET SO-8 package uses wires to connect the source and gate to the leads, but on the drain sides, the leads are directly connected with the die pad, as shown in Fig. 1b. Thermal behaviors between these two packages can be very different, which will be discussed later.

Fig. 1. Various types of SO-8 packages a: standard IC; b: standard power MOSFET; c: strap-bonded; d: leadless; e: strap-bonded with leadless.

In order to improve the thermal and electrical performance of SO-8 packages, a solid copper strap that covers the surface of the die is adopted to replace the wirebonds connecting source to the leadframe [5] (Fig. 1c). This provides highly conductive path in addition to the existing path through the die pad connected to the leads.

Thermal performance can be further improved by providing a direct path from the backside of the copper die attach pad to the board [6] (Fig. 1d). The main thermal path is through the large copper pad exposed on the bottom of the package, which improves thermal resistance dramatically. This package is usually called leadless package or microleadframe package (MLF).

In the following, all thermal results are obtained by using the FLOTHERM 3.1 simulation tool. Fig. 2 plots the junction-to-ambient thermal resistance [1] of different types of SO-8 packages (described in Fig. 1) with same die size and package dimension. We notice a huge difference in thermal resistance between the standard IC SO-8 and standard power MOSFET SO-8. The direct connection of the copper die pad to the leads in standard power MOSFET SO-8 provides a path for heat dissipation to reduce the junction temperature dramatically. Reduction of thermal resistance by using strap bonding is about 15.2% over the standard power SO-8 package, as shown in Fig. 2. When the leadless package format is adopted, the thermal resistance can be reduced to 52 °C/W. Fig. 2 suggests that even though the package dimension and chip size remain unchanged, thermal performance can be significantly improved by an appropriate package design and improved interconnect. For example, with an ambient temperature of 50 °C and 1 W power dissipation for the chip, the junction temperature with standard IC SO-8 package is as high as 201.8 °C. However, with leadless package, the junction temperature drops to 102.3 °C.

[1] The package is mounted on 1 in^2 of 2-oz copper on FR4. Same condition applies to the packages in Fig. 3.

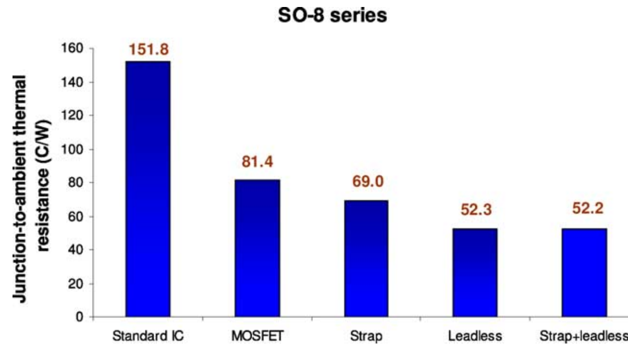

Fig. 2. Comparison of thermal resistances for various SO-8 packages.

The question remains if any further thermal benefit could be gained with the strap bonding applied to a SO-8 leadless package, as shown in Fig. 1e. Fig. 2 plots the simulation results compared to other types of power SO-8 packages. The improvement is almost negligible in comparison to leadless packages from a thermal point of view. The heat dissipation by the direct contact of copper pad to the board in leadless package is so dominant that heat dissipation through strap bonding is minimal.

Fig. 2 presents a clear picture how the package design affects the thermal behaviors. Comparisons of these packages reveal the fundamental cooling mechanism associated with the package design. Providing a direct path for the heat dissipation between chip and board can enhance the package thermal performance. When a package is designed such as leadless, in which the heat dissipation is maximized in one path, the improvement by additional heat path would be insignificant.

Now let's look at the flip-chip packaging application in power MOSFET devices, as shown in Fig. 3. The drain side in Fig. 3a is connected to the solder ball through the conduction layer, which is encapsulated by the epoxy-based materials. A full array of solder balls with 6×5 is assumed over the package. The heat can be dissipated through the solder balls directly beneath the chip and those connected to the drain side. Fig. 4 investigates the effect of the conduction layer on the thermal dissipation. It is interesting to note that, unlike the strap bonds used in SO-8 packages (Fig. 1c), where the copper strap improves thermal performance significantly, the conduction layer (copper) used in BGA as shown in Fig. 3a has negligible effect on thermal resis-

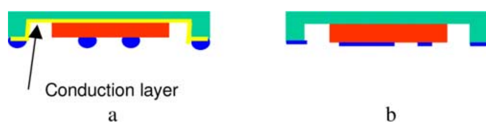

Fig. 3. a: Ball grid array (BGA) MOSFET package; b: large contact interconnect MOSFET package.

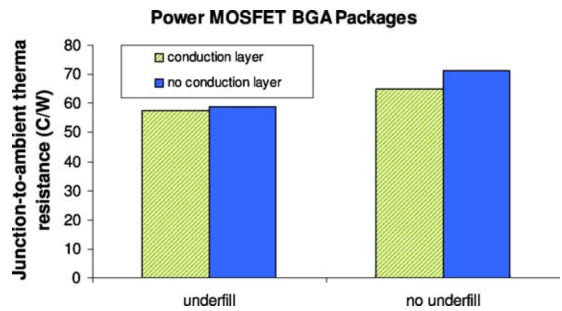

Fig. 4. Thermal resistance of full array BGA MOSFET packages.

tance. "No conduction layer" in Fig. 4 means that the conduction layer has very low thermal conductivity ($\sim$0.9 W/Km) which, of course, is not realistic. The results imply that the heat dissipation is dominant through the path of solder balls under the chip. Fig. 4 also shows the effect of underfill on thermal resistance. The improvement is about 12% reduction over the same package without underfill.

A ball grid array approach, even with multiple balls per connection has a limited contact area with a printed circuit board and hence the thermal performance from the junction to board and conduction efficiency can not be maximized. Therefore an underfill material is

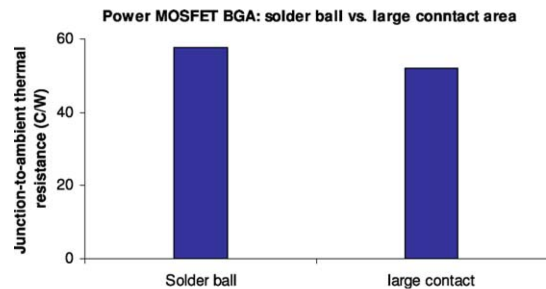

Fig. 5. Comparison of thermal resistance between BGA MOSFET and large contact area MOSFET package.

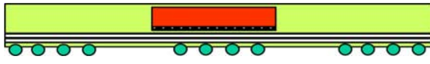

Fig. 6. A overmolded ball grid array (BGA) package with thermal balls.

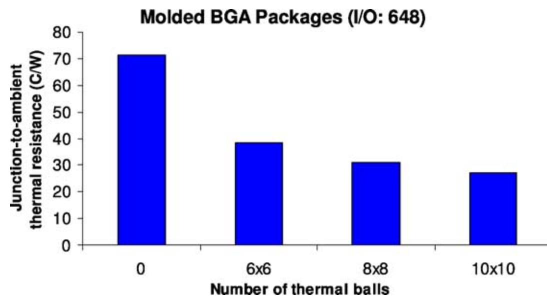

Fig. 7. Effect of thermal balls on thermal resistance for overmolded BGA package.

Fig. 8. a BGA package with an integrated heat-spreader.

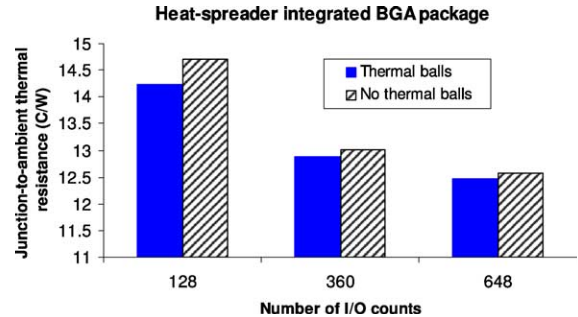

Fig. 9. Thermal resistances for heat-spreader integrated package.

required in the above applications. An alternate interconnection methodology [7] has been developed using a large area contact technique, as shown in Fig. 3b. Fig. 5 presents the results of thermal resistance for large contact interconnect compared to the BGA package discussed before. We notice a 10% reduction in thermal resistance over the BGA package. It is noted that the large contact area package does not require the underfill.

One of common techniques to improve the thermal performance of BGA packages is the implementation of thermal balls, as shown in Fig. 6 for a typical overmolded BGA package. The thermal balls, located on the center of package under the chip, provide a direct heat dissipation path. In order to understand the significance of the thermal balls, in Fig. 7, [2] the thermal resistance is plotted as function of the number of thermal balls. The package has 648 I/O counts. A single solder ball diameter is assumed to be 750 μm with 1.27 mm pitch. Fig. 7 clearly shows that the thermal balls have significant contributions to the reductions of thermal resistance. With 8×8 thermal balls, the resistance can be reduced more than 50% over the package without thermal balls.

In order to further improve the thermal performance of BGA packages, a copper spreader can be assembled on the top, as shown in Fig. 8. The spreader is then connected to the substrate through the stiffeners on the four sides of the package. In Fig. 9, the results of the thermal resistance for different number of the package I/O counts are plotted for the packages with and without thermal balls. Surprisingly, the thermal balls have almost negligible impact on the overall thermal performance over a wide range I/O number from 128 to 648. The simulation results show that the majority of the heat is dissipated through the top heat-spreader due to its high conductivity and large area. The heat is further conducted through the stiffeners, substrate, signal solder balls, and eventually will be dissipated by convection through the PCB board. The thermal balls, as the secondary heat dissipation path, therefore have insignificant effect.

[2] The package is mounted to 4-layer PCB board according to JEDEC standard. Same condition applies to the package in Fig. 8.

3. Optimal package design: combined thermal and mechanical modeling

Although the package thermal performance can be enhanced through thermal simulation, the improved package design must also be robust in various harsh environmental conditions (thermal cycling, high temperature/high humidity storage, soldering reflow etc.). Such conditions impose serious thermal stresses and other stresses (such as the vapor pressure by moisture vaporization, and the dynamic loading due to shock, etc.). Currently, 65% of all failures in microelectronics is related to thermo-mechanical problems [8]. This is expected to become even more critical in the future microelectronic products due to the continued trend of further miniaturization and function integration. Also, based on the root cause analyses of observed failures, most of the thermo-mechanical problems originate from the product and/or process design phase. Therefore, the importance of thermo-mechanical simulation in package

design has been long recognized in electronic packaging industries.

However, the mechanical design using the thermo-mechanical simulation tools is often carried out independently from the thermal design in packaging development phase. Sometimes, the mechanical simulation is applied when a thermal design is fixed. As a result, the package overall performance is not optimized both in mechanical and thermal aspects. Another concern is the reduction of thermal performance during operation cycling due to the reliability issues, such as the interface delamination and cracking, which will cause the excessive thermal contact resistance. Therefore, in order to achieve an optimized package design, the combined thermal and mechanical modeling are necessary. In the following, two thermally enhanced electronic packages are used to demonstrate the interactions and trade-off between thermal and mechanical designs.

3.1. A heat-spreader integrated ball grid array package

A flip-chip version of BGA package with a heat-spreader on the top, as shown in Fig. 8, is considered. The goldstud bumping is used as the interconnect between the chip and substrate. There have been concerns regarding the fatigue life of the Au bumps in comparison to the conventionally eutectic solder bumps. However, numerous studies have demonstrated that when the underfill is applied, the bumps are very robust and can meet the JEDEC thermal cycling specifications [9].

The board-level solder joint reliability is always one of the major concerns for BGA types packages. In the following, ANSYS 5.2 simulation tool is used for the thermo-mechanical analysis. A visco-plastic modeling of the solder joints subjected to the thermal cycling is carried out first to evaluate the fatigue behaviors of individual solder joints [10]. In Fig. 10, the maximum creep energy density is plotted against the location of solder balls. The solder ball with the largest creep energy density is susceptible to fail first during thermal cycling. Fig. 10 shows that the most outer thermal balls have much higher creep energy density than the most outer signal balls. This is because the local CTE mismatch between the silicon chip and the PCB board is much more than the local CTE mismatch between the plastic substrate and PCB board. Thus the thermal stresses of solder balls beneath the chip is expected to be much higher than the stresses on the outermost solder balls. Fig. 10 also shows that the introduction of thermal balls contributes a beneficial effect to the signal solder balls, but the reduction in creep density of solder balls is not significant.

As we may recall, thermal simulation results in last section show that the implementation of thermal balls for high density BGA packages with heat-spreader has almost negligible effect on the thermal performance. The

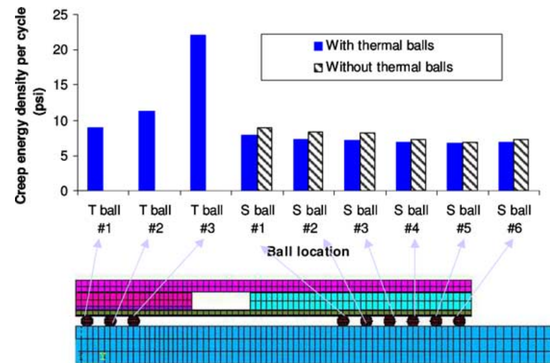

Fig. 10. Visco-plastic solder joint thermal cycling modeling results for a BGA package with an integrated heat-spreader.

mechanical simulation results above show that the thermal balls are less reliable (higher creep density) and also do not give significant improvement in signal solder balls' reliability. This seems to suggest that it is not necessary to add thermal balls from both thermal and reliability aspects. This conclusion, however, is not the final solution.

From Fig. 8, it can be seen that the thermal dissipation path of a heat-spreader integrated BGA package comes cross several interfaces, such as the interfaces at chip/spreader, spreader/stiffener, stiffener/substrate, substrate/solder balls and solder balls/PCB. The possible delaminations or cracking at these interfaces will contribute very high thermal contact resistance. This will degrade the thermal performance significantly. Let us consider an Au-stud bumped on flex BGA package, where a flex substrate is used to improve the electrical and thermal behaviors. Assume that a phase change material is applied between the chip and heat-spreader. A typical phase change material has a phase transition temperature at 50 °C, above which the material virtually gives no mechanical constraints between the spreader and chip. However, thermal contact can be maintained when the gap is less than the maximum thickness of phase change material (usually up to 2 to 3 mils). In order to predict the magnitudes of the gap induced by the thermal stresses during the heating process, a linear elastic modeling is conducted for the packages with and without thermal balls. The stress-free temperature is assumed to be 50 °C (phase transition temperature). The maximum temperature is 150 °C. Fig. 11(a) and (b) present the general package deformation patterns with and without thermal balls. Fig. 11(c) gives the results of the gap at interface as function of the distance from the center. Since flex substrate is very thin and easy to warp, the gap between the chip and heat-spreader induced by the thermal stresses may be large enough to separate the chip from the spreader. Fig. 11(c) shows that in the absence of thermal balls, the maximum gap value can

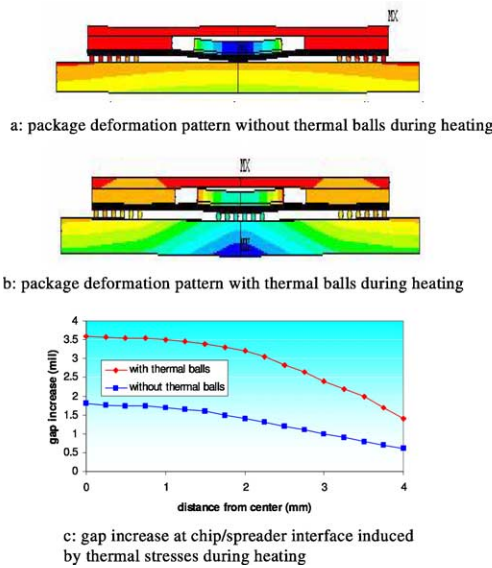

Fig. 11. Linear elastic finite element modeling of a BGA package with flex substrate and heat-spreader.

exceed 3 mil. Such a deformation may cause the non-contact at chip/spreader interface, thus overheating the chip. In addition, excessive flex substrate deformation with no thermal balls brings up the process issues of the package attachment onto the PCB.

In Fig. 12, a comparison was made for the thermal resistances of three cases: the package without delamination and thermal balls, the package with complete debonding at chip/spreader interface, but without thermal balls, and the package having delamination at chip/spreader, but with thermal balls. Fig. 12 shows that the delamination will lead a significant rise of thermal resistance. The introduction of thermal balls can reduce the impact of the delamination on the thermal performance by 15%. From Fig. 11, it also shows that the thermal balls can act as mechanical supports to reduce

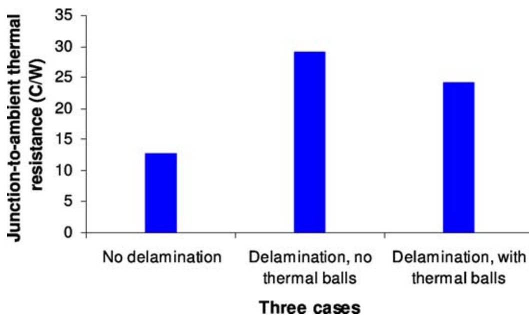

Fig. 12. Effects of the delamination and thermal balls on thermal resistance for a BGA package with an integrated heat-spreader.

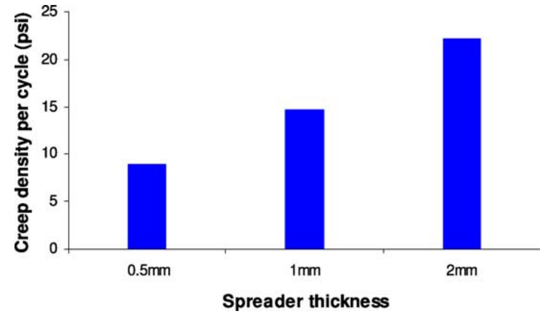

Fig. 13. Dependence of the creep density on spreader thickness.

the warpage of the flex, and at the same time, to reduce the gap between chip and spreader.

From the above analyses, it can be finally concluded that it is necessary to implement the thermal balls for this package. The thermal balls will provide the secondary heat dissipation path if there is any delamination in the primary heat dissipation path. Thermal balls also give the mechanical support to prevent the flex from the excessive deformation during the process and at the same time to reduce the gap between the chip and spreader. Besides, it is suggested from above analysis that the phase change material should not be used at chip/spreader interface when flex substrate is applied.

Next the impact of the heat-spreader thickness on the solder ball joint reliability is investigated. Although there is no direct connection between the solder balls and the spreader, the global CTE mismatch-induced thermal stresses will affect the fatigue behaviors of the solder balls. Fig. 13 plots the maximum creep energy density as function of spreader thickness. It shows that the increase of the spreader thickness will reduce the solder joint fatigue life.

On the other hand, thermal analysis indicated that the beneficial gain can be obtained when the spreader thickness increases. Therefore, there is a trade-off in determining the spreader thickness. An appropriate thickness can be selected based on the reliability requirement and thermal specifications.

Finally the effect of heat sink attachment on solder balls behaviors is considered. It is common practice that the thermal cycling test is done at a component-level without the heat sink attachment. But the additional heat sink attachment will induce the additional thermal stresses on the solder balls. Fig. 14 shows that the heat sink attachment can cause almost 100% increase of the creep density over the package without heat sink attachment. Again, an appropriate trade-off design must be considered between the thermal and mechanical performance. The selection of the interface materials at spreader/heat sink is important to minimize the impact of heat sink on solder joint stresses. The application of phase change material between the package and heat

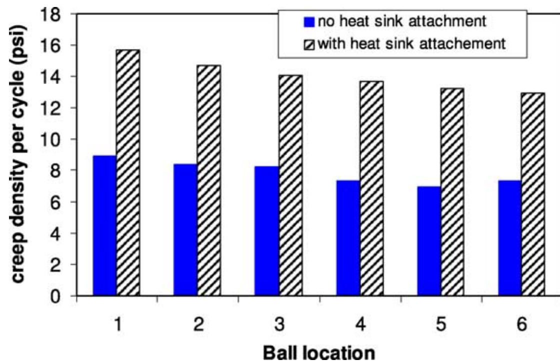

Fig. 14. Effect of heat sink attachment on the solder joint reliability.

sink is effective in reducing the global mismatch caused by the attachment, therefore would improve the solder joint reliability.

3.2. A bottomless standard outline package

For a standard outline package, the thermal performance can be maximized with an embedded heat sink, which provides a direct path from chip to board for the heat dissipation (e.g. See Fig. 1d). Fig. 15 shows the cross-section and bottom views of the package. Given the specifications of thermal requirements, the dimensions of the copper heat sink and the package dimensions can be determined through the thermal simulation. However, due to the large CTE mismatch between the encapsulant and copper, high thermal stresses are developed in the mold compound region adjacent to the embedded heat sink. Consequently, plastic cracking and delamination at the encapsulant/copper interface are often encountered and observed for such types of packages, as shown in Fig. 16. In order to protect the package from such failures, a careful thermal stress analysis should be carried out in the design phase, together with the thermal analysis.

One of issues for the thermal stress analysis is the selection of a meaningful and appropriate stress component, which has the major contributions to the failures. In a 3-dimensional stress analysis, there are six

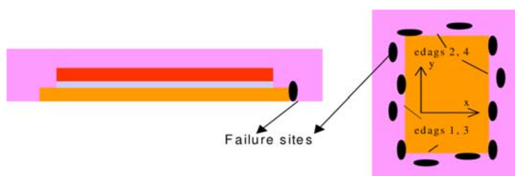

Fig. 15. Effect of heat sink attachment on the solder joint reliability.

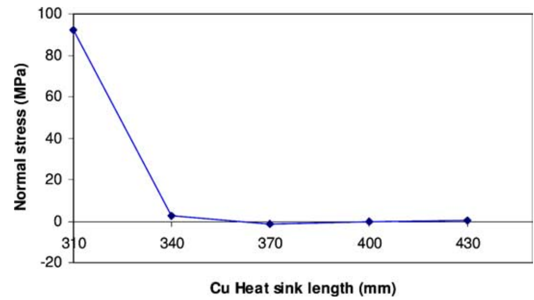

Fig. 16. Normal stress vesus Cu length.

stress components for each point. Besides, several effective or equivalent stresses such as principal normal and shear stresses, Von Mises stresses, mean stress and devitoric stresses are provided. The Von Mises stress is often used in stress analysis to represent the overall stress state of a particular location. However, such a selection does not always make sense.

For the cracking and delamination that are present on each side of the copper heat sink, the high tensile stress normal to the interface of copper/encapsulant is the major contribution to the failures. Compressive stress normal to the interface does not contribute to the delamination and cracking. Besides, the stress components other than that normal to the edge have insignificant effect on the failures. Therefore, in the following, we will use the normal stress (to the interface) to analyze the cause of the failures. The Von Mises stress is also given for the comparison and discussion purpose. Caution should be made in selecting the normal stress in each edge, under the unified global Cartesian coordinate system. For example, in Fig. 15, σ_x represents the normal stress for edge 1 and 4, but σ_y represents the normal stress for edge 2 and 3.

In finite element modeling, the element size should be controlled at a fixed value for different package configurations throughout the study, to minimize the local stress singularity problem. As we know, the stress singularity is present in each interface and crack tips [9]. This means that the stress is very much dependent on the local element size to be taken. A fracture mechanics approach can solve the singularity problems but much more complicated. Therefore in the present analysis, a linear stress analysis is applied with fixed element size at the point of interest.

In Fig. 16 the normal stress along one edge is plotted as function of copper length in perpendicular direction. It is interesting to note that when the copper length is in the range between 310 and 340 mm, high tensile stress is developed at this location. However, when the copper length increases further, the normal stress is nearly zero or becomes compressive. Such a result implies that it is very important to select an appropriate copper length in

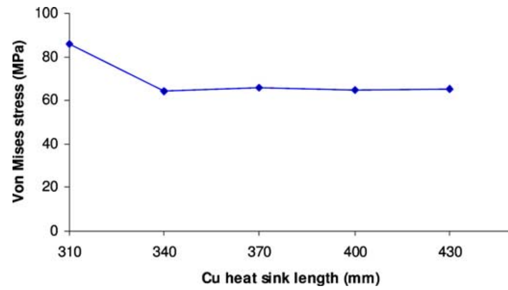

Fig. 17. Von Mises stress vesus Cu length.

the thermal analysis to ensure that the selected geometry avoids the high tensile stress range.

As a comparison, in Fig. 17 the Von Mises stress is plotted at the same location. Although Von Mises stress exhibits the similar trends to the normal stress in Fig. 16, it is hard to tell whether the stress is positive or compressive from the Von Mises stress plot.

The accuracy of the linear thermal-stress analysis is always a concern in thermo-mechanical modeling. Inaccurate material properties of Young's modulus and CTE, and other unknown factors, such as the chemical shrinkage and the exact stress-free conditions often lead to the opposite predictions compared to the experimental observation. For example, the warpage analysis of a package by a linear elastic analysis somehow often contradicts to the measurement results, due to the chemical shrinkage effect. This implies that it is very important to verify whether or not our simulation results make sense.

In order to do so, a sweeping analysis over a wide range of CTE of mold compound is given in Fig. 18, in which the copper length is selected as 350 mm according to the previous analysis. It shows that the normal stress changes in a very narrow range of stress level from −5 to 5 MPa, regardless of the change of mold compound CTE. This indicates that given the consideration of the inaccuracy of CTE input, the selection of the copper length based on the Fig. 16 I still valid. The normal

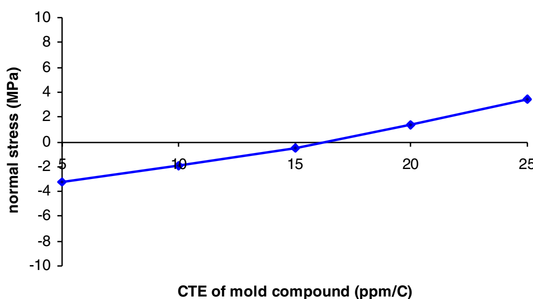

Fig. 18. Dependence of normal stress on CTE of mold compound.

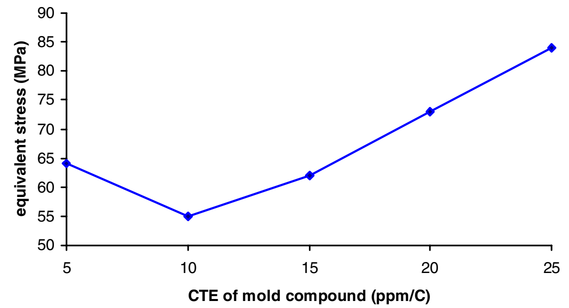

Fig. 19. Equivalent stress versus CTE of mold compound.

stress always remains in a very low level and is not sensitive to mold compound CTE.

Fig. 19 plots the Von Mises stress of the package over a wide range of CTE of mold compound. It shows that Von Mises stress is sensitive to the CTE. Fortunately, as discussed before, it is not appropriate to use Von Mises stress for this problem.

Therefore, we conclude that our designs of the heat sink dimensions based on the normal stress analysis can be justified, and hence are acceptable. Indeed, our DOE experiments confirmed and agreed well with our analysis.

4. Vapor pressure modeling: analysis for moisture-induced failures

Moisture-induced failure does not only occur in the electronic packaging field but also in other engineering fields (fiber reinforced composites, concrete, etc.). Such a problem is often referred to as a 'popcorn' failure. The 'popcorn', however, actually originates from the delamination and rapid propagation of delamination along the critical interfaces in packages, due to the combination of high vapor pressure and the degradation of the adhesive strength by the moisture at reflow temperature [11–13]. Therefore, it is important to model the vapor pressure distributions and variations with temperature and moisture absorption.

Let's first estimate the amount of moisture absorbed by a typical plastic material. Consider a plastic material in 85 °C/85 RH ambient moisture conditions. A typical value of the saturated moisture concentration, C_{sat}, is $1.25e^{-2}$ g/cm^3 [14]. The physical meaning of the C_{sat} is the moisture density over the *total* material volume. A comparison can be made for C_{sat} to the ambient moisture (vapor) density at 85 °C/85 RH, i.e., $\rho_{ext} = 0.85\rho_g = 3.04\ e^{-4}$ g/cm^3, where ρ_g is the saturated vapor density at 85 °C. It is straightforward to note that $C_{sat} = 41\rho_{ext}$! This implies that the most amount of moisture in material must be condensed into the liquid form. The moisture in material hence is in the mixed

liquid/vapor phase. In fact, the diffusion process of moisture is the transport process of moisture from ambient to material inside by moisture condensation. The moisture will stay in micropores or free spaces in material.

The C_{sat} is an 'apparent' moisture density, as it is defined over the total material volume. Without loss of generality, we may assume that 95% of plastic material is solid, which means only 5% of total volume is micropores or free spaces. Thus the 'real' moisture density in material, denoted as ρ, is $\rho = 820\rho_{ext}$! This number clearly shows how much moisture a typical plastic material could absorb. Obviously, the 'real' moisture density in *voids* can never exceed the water density at that particular temperature in preconditioning. Besides, it is obvious to note that the vapor pressure in the plastic material is not equal to the ambient vapor pressure at pre-conditioning, as shown in Fig. 20.

A vapor pressure model has been developed based on a microvoid approach [15–18]. The whole-field vapor pressure finite element modeling has been conducted for various packages [19]. The desorption of the moisture during the reflow is also considered. One of the main conclusions from the modeling results is that the maximum vapor pressure at reflow is not always proportional to the moisture absorption. For example, at reflow temperature 220 °C, the saturated vapor pressure is 2.32 MPa. If the moisture is not fully vaporized at reflow, the vapor pressure will maintain the saturated value no matter how much moisture is absorbed.

The growth and coalescence of microvoids near interfaces is recognized as the precursor to interface delamination [18]. The interface delamination not only depends on the vapor pressure, but also on the interface strength as well. When the vapor pressure maintains its saturated value, the interface strength becomes a key factor for the delamination.

The correlation between the interface strength and moisture absorption is very complicated. Some materials exhibit the excellent resistance to the moisture absorption, while some materials' interface strength is very sensitive to the moisture absorption. Therefore, based on the vapor pressure modeling and the above analysis, it can be concluded that the amount of moisture absorption does not have direct correlation with failures. Some failures may occur for the materials with less moisture absorption, since the adhesion of these materials is weakened significantly with moisture absorption. Some materials do not fail, even with more moisture due to the excellent resistance of interface strength against the moisture and temperature. For *same* material, however, there is direct correlation between the delamination and the moisture absorption.

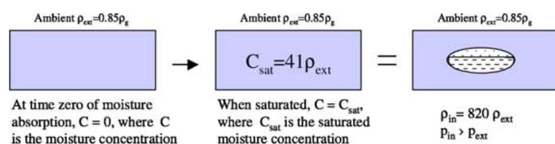

Fig. 20. Moisture absorption for a typical plastic material at 85 °C/85 RH.

Therefore, the interface adhesion after moisture absorption at high temperature becomes one of most important indicator to identify the failures. It is not appropriate to use the moisture absorption as criterion to evaluate the material's performance at reflow. The vapor pressure modeling is helpful for us to understand the mechanism of moisture-induce failures.

The question remains that if the void growth is considered, how to estimate the vapor pressure during the void growth and after the delamination is formed. A consistent model has been given by the microvoid approach and three distinct cases have been identified [18].

5. Summary

This paper discusses the roles of thermal and thermomechanical simulation in the design of electronic packages. An appropriate thermal design using thermal simulations can make a package to achieve better thermal performance, with even smaller chips and package dimensions. However, thermal modeling has to be combined with thermomechanical modeling to ensure the final design is robust and reliable. A trade-off must be considered in thermal and mechanical performance. The thermal and mechanical modeling (including vapor pressure modeling) are also very useful in providing necessary information and criterion for the materials selection prior to prototyping.

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